

## **REMARKS**

This paper is filed in response to the Office Action dated November 2, 2005. As this paper is filed on February 2, 2006, this paper is timely filed.

### **I. Status of Amendments**

Claims 1-17 were previously pending, claims 16 and 17 having been withdrawn as a consequence of applicant's Response to the restriction requirement of August 5, 2005. By this amendment, claims 1-15 have been amended. Consequently, claims 1-17 remain pending, with claims 16 and 17 withdrawn.

### **II. Response to the November 2 Office Action**

The abstract is objected to as being more than a single paragraph, and including limitations of the non-elected claims. The abstract has been amended, and, based on this amendment, applicant requests that the objection be withdrawn.

Claims 1 and 12 are objected to for informalities. Claims 1 and 12 have been amended as suggested on the top of page 3 of the November 2 Office Action, and, based on this amendment, applicant requests that the objections be withdrawn.

Claims 1-9 and 12-15 are rejected under 35 U.S.C. 102(b) as being allegedly anticipated by Morita et al. (U.S. Patent No. 6,335,901). Claims 10 and 11 are rejected under 35 U.S.C. 103 as being obvious in view of the combination of Morita et al. and Luk et al. (U.S. Patent No. 5,883,814). Applicant has amended claim 1, and responds as follows.

Claim 1, as amended, recites a process for designing semi-conductor memory components. The process includes: designing of a first layout for a semi-conductor memory module of the semi-conductor memory component to be used for a first configuration of the semi-conductor memory component; designing of a second layout for the semi-conductor memory module to be used for a second configuration of the semi-conductor memory component, the second layout being different from the first layout; using the first layout or

the second layout for the total layout of the semi-conductor memory component, depending on the particular configuration of the semi-conductor memory component, together with at least one further layout for at least one further semi-conductor memory module of the semi-conductor memory component that is identical and not dependent of the particular configuration of the semi-conductor memory component. The first and second layouts for the semi-conductor memory module have essentially the same external dimension and are arranged at the same locality of the total layout.

In particular, applicant notes that amended claim 1 recites that the second layout is *different* from the first layout. Further, the first layout or the second layout is used together with at least one further layout for at least one further semi-conductor memory module of the semi-conductor memory component which is identical and not dependent on the particular configuration of the semi-conductor memory component. Additionally, the first and second layouts have essentially the same external dimensions and are arranged at the same locality of the total layout.

By comparison, that section of Morita et al. relied upon in the November 2 Office Action relates to the activation and deactivation of a clock regeneration circuit 3. According to col. 13:1-15, the clock regeneration circuit 3 may be deactivated under certain conditions (SDR-spec). According to col. 13:28-31, the clock regeneration circuit 3 may be activated under other conditions (DDR-spec). In any event, Morita et al. discusses a single circuit that may be selectively activated or deactivated.

As such, to the extent the clock regeneration circuit 3 allegedly corresponds to the first or second layout, it cannot be both, for the first and second layouts are claimed to be *different* from each other. Rather, the clock regeneration circuit 3 is *a single circuit* that may be selectively activated or deactivated according to the desire of the user. Consequently, the clock regeneration circuit 3 cannot meet the remainder of the limitations of the claims, such as the limitation that the first and second *different* layouts have essential the same external dimensions or may be arranged in the same locality.

As such, Morita et al. does not disclose each and every limitation of the claimed subject matter. As Mortia et al. does not disclose each and every limitation of the claimed

subject matter, Morita et al. does not anticipate the subject matter of claim 1. Consequently, the rejection should be withdrawn.

As to the rejections of claims 2-15, applicants note that claim 1 is not anticipated by Morita et al., for the reasons provided above, that claims 2-15 depend from claim 1, and that any rejection of these claims not based solely on Morita et al. relies on Morita et al.'s application to claim 1. However, as claim 1 is allowable over Morita et al., claims 2-15 should also be allowable at least for the reason that they depend from claim 1. Consequently, all the outstanding rejections should be withdrawn.

### **III. September 7 Information Disclosure Statement**

On September 7, 2004, applicant submitted an Information Disclosure Statement (IDS) to the Office. A review of the PAIR system reflects that an IDS was received on September 9, 2004, and a review of the IFW reflects that the IDS received on September 9, 2004 was indeed the IDS mailed on September 7. However, an initialed copy of the Form PTO-1449 (modified) attached to the September 7 IDS was not attached to the November 2 Office Action to indicate that the examiner had reviewed the references listed thereon. Consequently, applicant respectfully requests that the initialed copy of the Form PTO-1449 (modified) from the September 7 IDS be included with the next paper to be issued by the Office.

In view of the foregoing, it is respectfully submitted that the above application is in condition for allowance, and reconsideration is respectfully requested. If there is any matter that the Examiner would like to discuss, the Examiner is invited to contact the undersigned representative at the telephone number set forth below. The Director is hereby authorized to charge any deficiency in the fees filed, asserted to be filed or which should have been filed herewith to our Deposit Account No. 13-2855, under Order No. 30169/30000. A duplicate copy of this paper is enclosed.

Dated: February 2, 2006

Respectfully submitted,

By 

Paul C. Craane

Registration No.: 38,851

MARSHALL, GERSTEIN & BORUN LLP

233 S. Wacker Drive, Suite 6300

Sears Tower

Chicago, Illinois 60606-6357

(312) 474-6300

Attorney for Applicant